LIST OF CLAIMS

The list of claims provided below replaces all prior versions and lists of claims in the application. Claims 1, 2, 5, and 7-9 are currently amended. Claim 6 is canceled. Claims 10–13 are new. Thus, claims 1-5 and 7-13 are pending.

Please amend the claims as follows.

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1. (currently amended) A processor comprising:

at least one register file;

at least one execution unit;

~~said at least one register file operatively connected to said at least one execution unit~~

at least one bypass circuit operatively coupled to said at least one register file and said at least one execution unit, said at least one bypass circuit capable of arbitrating access to said at least one register file; and,

a backing register file operatively coupled to said at least one register file, and where said backing register file is operationally and responsively coupled to at least one user-visible instruction.

2. (currently amended): A processor as in claim 1 further comprising a plurality of register files and further comprising at least one execution unit operably connected to each register file of said plurality of register files, and where said backing register file is operably connected to each register file of said plurality of register files providing thereby the ability to transfer values from any designated location in any designated register file of said plurality of register files to any designated location in said backing register file, and from any designated location in said backing register file to any designated location in any designated register file of said plurality of register files.

3. (original): A processor as in claim 1 further comprising a connection circuit having a first connection and a second connection, where said first connection is operably connected to said backing register file and said second connection is operably connected to a main memory.

4. (original): A processor as in claim 2 further comprising a connection circuit having a first connection and a second connection, where said first connection is operably connected to said backing register file and said second connection is operably connected to a main memory.

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5. (currently amended): A method for moving values from designated locations in designated register files to designated locations in a backing register file and values in designated locations in said backing register file to designated locations in designated register files comprising:

(a) identifying a backing register file instruction in a sequence of instructions;

(b) decoding said backing register file instruction, where if said backing file instruction is one of load-backing-register-file or load-register-file, making available addresses for specified numbers of locations in specified register files and an equal number of addresses for specified locations in said backing register file, where said number of addresses is at least one~~, if said backing file instruction is one of load-backing-register-file or load-register-file~~;

(c) reading values from each of said addresses in said specified register file and writing said values to said equal number of addresses in said backing register file as specified by said backing register file instruction, if said backing register file instruction is of type load-backing-register-file; and,

~~(c)~~ (d) reading values from each of said addresses specified in said backing register file and writing said values to said equal number of addresses in said specified register file, if said backing register file instruction is of type load-register-file.

6. (canceled).

7. (currently amended): A ~~machine~~ computer readable medium containing ~~a~~ ~~data structure having~~ a backing register file instruction ~~therein~~.

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8. (currently amended): A ~~machine~~ computer readable medium ~~containing a data structure~~ as in claim 7 further comprising ~~a~~ the backing register file instruction for transferring register values between a register file and said backing register file.

9. (currently amended): A ~~machine~~ computer readable medium ~~containing a data structure~~ as in claim 7 further comprising ~~a~~ the backing register file instruction for transferring values between main memory and said backing register file.

10. (new): A computer readable medium of claim 7 further comprising a set of instructions for a singly linked list and a byte stream, wherein the singly linked list and the byte stream contain backing register instructions.

11. (new): A processor of claim 1 further comprising the backing register file capable of being explicitly used by programs at all privilege levels.

12. (new): A method of accessing a backing register file comprising:
identifying a backing register file instruction in an instruction stream;
switching modes to access a backing register file; and
moving values between a main memory and a backing register file.

13. (new): A method of claim 12 further wherein one mode emulates a legacy software.